IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

6/B P.Walls 2.3-03

Applicant(s): Mahajani et al.

Application No.:

10/079472

Filed: February 19, 2002

Title: Gate Dielectric Structures for Integrated Circuits and Methods for Making and Using Such Gate Dielectric Structures

Attorney Docket No.: 40025.005,

(MA-068)

Group Art Unit: 2814

Examiner: Thao X Le

FAX RECEIVED

JAN 2 2 2003

TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents

Washington, D.C. 20231

AMENDMENT AND RESPONSE

Status of Claims:

Claims 1-26 have been rejected under 35 USC 103.

AMENDMENT

Please enter the following amendment and remarks in response to the Office Action of October 22, 2002.

IN THE SPECIFICATION

Please amend paragraph [37], on page 11, as follows. Appendix A contains a marked-up version of this paragraph showing the changes being made.

[37] The gate oxide of the TFT device is made in the invention using substantially the same ISSG process described above (i.e., that described for SONOS

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B) end

devices) except that for TFT devices, the oxide is grown over polysilicon. Thus, the growth rates will be more than the growth rates described above for SONOS devices. Accordingly, lower process temperatures and/or shorter times will be required for TFT devices to obtain a similar oxide thickness as SONOS devices. In one aspect of the invention, the temperature for the ISSG process used to make the gate dielectric for TFT devices can range from about 600 to about 900 degrees Celsius, preferably about 700 to about 850 degrees Celsius, and more preferably about 800 degrees Celsius.

IN THE CLAIMS

Please cancel claims 2, 4, 10, 11, and 16-19 without prejudice. Please amend claims 1, 3, 5, 8-9, and 20-26 as follows. Please add new claims 27-34. All pending claims are provided in clean form, beginning on the next page. Appendix B contains a marked-up version of these claims showing the changes made.

PTO/SB/17 (01-03)

Approved for use through 04/30/2003. OMB 0651-0032
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Applicant Claims small entity status. See 37 CFR	1.27					TEO! III				
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Name (Print/Type) Pamela . Squyres	(A	потву/Ад	ent)	5224	<u> </u>		Teleptione Date		869-2921	

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Matrix Semiconductor, Inc. 3230 Scott Boulevard Santa Clara, California 95054 Telephone 408.969.4848 Facsimile 408.969.4849

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Time:	(Santa Clara, California)							
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	FAX NUMBER 703-308-1	7722	JAN 2 2 2003					
* Please deliver to Examiner Thao X. Le in Art Unit 2814. * Document(s) Transmitted: Fax Cover Sheet (1 pg) Power of Attorney (1pg) Statement Under 37 CFR 3.73(b) (1pg) Fee Transmittal in duplicate (2 pgs) Amendment and Response to Office Action of 10/22/02 (23 pgs)								
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	In re. Patent Application of: Maitreyee Mah.	ajani et al. Ex	aminer: Thao X. Le					
	Serial No.: <u>10/079472</u>	Gro	oup Art Unit: <u>2814</u>					
	Filed: February 19, 2002	Do	cket No.: <u>MA-068</u>					
	Title: Gate Dielectric Structures for Integra Such Gate Dielectric Structures	By: (Pamela J. Squyres Jo.: 52,246					
1 hereb	by certify that this paper is being transmitted t	by facsimile to the l	U.S. Patent and Trademark Office					